REMARKS

Claims 44-73 are presently pending. Claims 44-47, 49-52, 54, 56-61, 63, 65-69, 71 and 73 are rejected. Claims 48, 53, 55, 62, 64, 70, and 72 are objected to but were indicated as allowable if rewritten in independent form. Assignee appreciates Examiner's indication of allowable subject matter.

Claims 44, 49, 57 and 66 were rejected under 35 U.S.C. 103(a) as obvious from Shaik and obvious from Azuma. Among the criteria for a rejection under 35 USC 103(a), "the prior art reference (or references when combined) must teach or suggest all the claim limitations." MPEP 2143.

Shaik notes that "By configuring NOT comparator circuit 301 and TRUE comparator circuit 302 in parallel to enable a respective one or the other of the redundant row predecode circuit 204a and a normal row predecode circuit 204b, the redundancy logic configuration of Fig. 3 eliminates comparator-related setup and hold time constraints on timing of row addressing paths (including e.g., predecode and decode circuits) of a semiconductor memory array or subarray such as memory block 200." Shaik, Col. 6, Lines 6-14.

Claims 44, 49, 57, and 66 recite, among other limitations, "shifting" in/out a "predecoder". Examiner has indicated that "Shaik clearly shows a method and structure for providing memory redundancy by either selecting the redundant predecoder (204a) when the failed address register indicating a failed address or selecting the normal predecoder (204b) when the failed address register does not indicate so. In this way, though the reference does not specifically spelled out the word "shifting in/out predecoder" as claimed, it would be obvious to one skilled in this art than when one decoder is selected, it must be shifted into its use, and then the other must be deselected or shifted out of its useful work as well." Office Action, p. 2.

As an initial matter, Examiner characterization of Shaik does not provide a basis for concluding that "it would be obvious to one skilled in this art that when one decoder is selected, it must be shifted into its use, and then the other must be deselected or shifted out of its useful work as well".

Moreover, respectfully submits that Shaik does not teach or fairly suggest "shifting" in/out a "predecoder". "As noted above, Shaik teaches "configuring NOT comparator circuit 301 and TRUE comparator circuit 302 in parallel to enable a respective one or the other of the redundant row predecode circuit 204a and a normal row predecode circuit 204b … " Shaik, Col. 6 Lines 6-9 (Emphasis Added). Thus, in Shaik, "when one decoder is selected", it is not shifted, and when the other is be deselected, it is not shifted out.

Accordingly, for at least the foregoing reasons, Assignee respectfully traverses the rejections to independent claims 44, 47, 57, and 66, as well as to dependent claims 45, 46, 50-52, 54, 56, 58-60, 67, 68, 70, and 72 as obvious from Shaik, and request that Examiner withdraw the rejections.

Claims 44-47, 49-52, 54,56-61, 63, 65-70 & 72, were also rejected as obvious from Azuma. Examiner has indicated that "Azuma (see Fig. 5) clearly shows a method and structure for providing memory redundancy by either selecting right predecoder (404) when the failed address register indicating a failed address or selecting the normal predecoder (402) when the failed address register does not indicate so."

Assignee respectfully submits that Azuma Figure 5 does not have any reference numeral 305a, 305b, 307, 310a, 310b, 318a, 410a, 402 or 404, "failed address register", "right predecoder", and accordingly traverses all the rejections based on Azuma. In fact, the reference numerals cannot be found in the reference, at all. It is believed that the Azuma reference was erroneously identified as the basis of the rejection. To the extent that

Examiner intended to reject claims based on Azuma, Assignee is unable to ascertain the basis for the rejections from the explanation in the present Office Action and requests that the basis be explained in a non-final office action.

Additionally, claim 44 recites, among other limitations, "shifting out at least one first predecoder of a plurality of first decoders". Claim 49 recites, among other limitations, "identifying at least one first predecoder of a plurality of first predecoders".

Shaik, Figure 3 shows ONE "Normal Row Predecode 204b" and ONE "Redundant Row Predecode 204a". Even if Examiner's characterization was correct, Shaik does not teach or fairly suggest "shifting out at least one first predecoder of a plurality of first predecoders". Thus, for at least the foregoing reasons, Assignee respectfully traverses the rejection to independent claims 44 and 49 and requests that Examiner withdraw the rejection to independent claims 44, and 49, and to dependent claims 45-48, and 50-56.

Claims 45, 50, and 59 recite, among other limitations, "shifting predecoded lines coupled to at least one of said first and second/said at least one other predecoder". Examiner has indicated that Shaik, "Fig. 3 shows that predecode address lines coupled to the shifting circuitry (301, 302) for shifting these lines into either the left predecoder (204a) or into the right predecoder (204b) as claimed." Assignee respectfully submits that Shaik, Figure 3, 301 and 302 merely provide enable signals to predecoders 204a, 204b. Comparators 301, 302 are not "shifting predecoded lines". Accordingly, Assignee respectfully traverse the rejection to claims 45, 50, and 59, as obvious from Shaik.

Claims 46, 51, 60, and 68 recite, among other limitations "shifting circuitry". Assignee respectfully submits that "shifting circuitry" does not read on the comparators 301, 302,

in Shaik. Accordingly, Assignee respectfully traverses the rejections to claims 46, 51, 60, and 68 as obvious from Shaik.

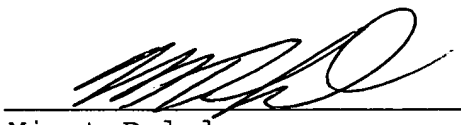
Conclusion

For at least the foregoing reasons, each of the pending claims are allowable. A notice of allowance is respectfully requested.

Commissioner is hereby authorized to charge any fees associated with executing any action requested herein.

Dated: July 14, 2006

Respectfully submitted,



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